What is claimed is:

1. A semiconductor memory device with an improved redundancy scheme, comprising a plurality of memory banks,

wherein each of the plurality of memory banks comprises:

normal memory cells arranged according to a row and column matrix structure; and

at least one redundancy line to be replaced with a defective line,

wherein the defective line is replaced with a redundancy line of a memory bank to which the defective line belongs, and the number of the redundancy line is set to be different according to the position of a memory bank including the redundancy line.

2. The semiconductor memory device of claim 1, wherein at least one memory bank, adjacent to an edge of photo shot, among the memory banks includes M redundancy lines and each of the other memory banks includes N redundancy lines (N is a natural number more than 1),

wherein M is a natural number that is larger than N.

3. The semiconductor memory device of claim 1, wherein at least one memory bank, adjacent to an edge of chip, among the memory banks includes M redundancy lines and each of the other memory banks includes N redundancy lines (N is a natural number more than 1),

wherein M is a natural number that is larger than N.

4. The semiconductor memory device of claim 1, wherein a row redundancy method is adopted.

5. The semiconductor memory device of claim 1, wherein a column redundancy method is adopted.

6. A semiconductor memory device with an improved redundancy scheme, comprising at least one memory block including a plurality of memory banks arranged in a column direction,

wherein each of the plurality of memory banks comprises:

a plurality of normal memory cells that are arranged according to a row and column structure; and

at least one redundancy line to be replaced with a defective memory cell,

wherein at least one memory bank, adjacent to an edge, among the plurality of memory banks, includes more redundancy lines than the other memory banks.

7. The semiconductor memory device of claim 6, wherein the edge indicates an edge of photo shot, and

at least one memory bank, adjacent to the edge of photo shot, among the plurality of memory banks includes M redundancy lines and the other memory banks includes N redundancy lines (N is a natural number more than 1),

wherein M is a natural number that is larger than N.

8. The semiconductor memory device of claim 6, wherein the edge indicates an edge of chip, and

at least one memory bank, adjacent to the edge of chip, among the memory banks includes M redundancy lines and the other memory banks includes N redundancy lines (N is a natural number more than 1),

wherein M is a natural number that is larger than N.

9. The semiconductor memory device of claim 6, wherein a row redundancy method is adopted.

10. The semiconductor memory device of claim 6, wherein a column redundancy method is adopted.